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DOCUMENT-IDENTIFIER: US 6307408 B1
TITLE: Method and apparatus for powering down a line driver

Abstract Text (1):
Various exemplary aspects of the present invention provide methods and apparatus for powering down the line driver to a state that reduces power dissipation without affecting the overall impedance of the line driver. More particularly, a power down state for line drivers and the like is suitably provided that saves power when no transmission is required. The power down mode suitably provides line termination for received data. According to various aspects of an exemplary embodiment, output devices are configured at power down such that a low impedance is maintained.

Brief Summary Text (2):
The present invention relates, generally, to methods and apparatus for creating a power down state in a circuit. More particularly, the present invention relates to a technique for powering down a line driver in a bidirectional transceiver while maintaining matched impedance without static power consumption.

Brief Summary Text (4):
Communications devices such as modems, cable modems, digital subscriber line (DSL) modems and the like are becoming increasingly common. Such devices typically facilitate data communications between a source and a destination across a communications medium such as a telephone line, coaxial cable, twisted pair cabling, copper wires, fiber optics, radio frequency (RF), infrared or other wireless interface, or the like. Generally, such communications are bi-directional in that both source and destination are allowed to transmit and receive data over the same medium.

Brief Summary Text (7):
Further, it is generally desirable to conserve power in line driver 150 whenever possible. One technique for reducing overall power consumption involves powering down line driver 150 when device 102 is not transmitting on medium 104. For reasons that will become apparent, it has been generally difficult to power down line driver 150 without affecting impedance Z.sub.LD. Hence, the driver impedance Z.sub.LD of many prior art systems did not adequately match the impedance Z.sub.line of communications medium 104 during power-down mode even if the impedance's properly matched when the line driver was powered up.

Brief Summary Text (10):
Various exemplary aspects of the present invention provide methods and apparatus for powering down the line driver to a state that reduces voltage drop without affecting the overall impedance of the line driver. More particularly, a power down state for line drivers and the like is suitably provided that saves power when no transmission is required. The power down mode suitably provides line termination for received data. According to various aspects of an exemplary embodiment, output devices are configured at power down such that a low impedance is maintained.

Detailed Description Text (8):
With reference now to FIG. 3, one technique for powering down line driver 150 suitably involves turning off both transistors 122 and 124. To turn off PFET 122, the gate terminal is wired "high", for example by connecting the gate terminal to the bias voltage 120. Similarly, NFET 124 may be turned off by connecting the gate terminal to a "low" input, such as by grounding the terminal. One technique for accomplishing a power down according to this technique is to connect the gate terminal of PFET 122 to a bias voltage 120 through a connection 310 and switch 306.

Similarly, the gate terminal of NFET 124 may be connected to ground though, for example, connection 312 and switch 308. Switches 306 and 308 suitably receive control signal 304 provided by a digital interface 302. Switches 306 and 308 may be any type of switch including any type of FET transistor, BJT transistor, electrical switch, relay or the like.

Detailed Description Text (11):
An improved embodiment for powering down line driver 150 suitably involves switchably connecting the gate terminals of PFET 122 and NFET 124 to the bias voltage V.sub.DD 120 during power down mode such that PFET 122 is turned "off" but NFET 124 is driven "on". With reference now to FIG. 4, NFET 122 remains connected to bias voltage 120 through connection 310 and switch 306, as appropriate. JFET 122 may be connected to bias voltage 120 though connection 404 and switch 402, which suitably receives control signal 304. When power down mode is indicated by control signal 304, switches 306 and 402 may be closed such that PFET 122 is off and NFET 124 remains on. Such an arrangement suitably creates an open circuit between the source and drain terminals of PFET 122 such that output voltage 116 may be isolated from bias voltage 120. As NFET 124 is turned on, a short circuit condition is created between the source and drain terminals of the transistor, thus shorting the output voltage 116 to ground, a low impedance condition. When output voltage 116 is shorted to ground, no static power is dissipated by transistors 122 and 124, so power consumption is effectively reduced. Moreover, a low impedance condition on output line 116 may be created and maintained such that line driver impedance Z.sub.LD remains approximately matched to the line impedance Z.sub.line, thus reducing noise and reflections in received signals.

CLAIMS:

10. A method of powering down a line driver, the method comprising the steps of:

providing said line driver, said line driver comprising at least two output transistors;

coupling each of said at least two output transistors to a reference voltage via at least two switches, each of said at least two switches being associated with one of said at least two output transistors; and

providing a control signal to each of said at least two switches such that said reference voltage is provided to each of said at least two output transistors such that one of said at least two output transistors is turned on and another of said at least two output transistors is turned off when said line driver is in a power-down mode.